depositing electrically conducting material in at least one of said blind vias wherein said electrically conducting layer is in electrical contact with said electrically conductive material in said at least one blind via;

removing portions of the layer of electrically conducting material to define a pattern of circuitry;

stacking a plurality of said sub-composites;

aligning said plurality of sub-composites;

B1 joining said plurality of sub-composites such that the electrically conducting material in at least one of said blind vias makes electrical contact by forming a metallurgical bond to the conductive pattern on an adjacent sub-composite; and

filling spaces between adjacent sub-composites with electrically insulating material.

B2 21. The method according to claim 20, wherein the electrically conducting material is deposited in at least one of the at least one passage through the dielectric layer by plating and the plating is electroplating or electroless plating.

B3 37. The method according to claim 1, wherein forming a metalurgical bond comprises heating the structures to a temperature above a melting point of at least one of the constituent of, or the cap deposited on, the electrically conducting material deposited in the at least one passage in the dielectric layer.

---

46. A parallel joining technology multi-layer electronic structure, comprising:

at least two substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the

B4 top surface or the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conductive material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by means of a metallurgical bond to one of the electrically conductive material filling the at least one passage and the circuitry pattern on another substructure; and

B4 cont'd electrically insulating material substantially filling a space between facing substructures except between a joined filled passage and circuitry pattern.

66. A parallel joining technology electronic package, comprising:

a multi-layer structure comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting material, the at least two substructures being stacked on each other such that one of the electrically conducing material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by a metallurgical bond to one of the electrically conducting material filling the at least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and a semiconductor chip attached to the multi-layer structure.

B5

67. (Amended) A parallel joining technology electronic package, comprising:

a printed wiring board comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by a metallurgical bond to one of the electrically conducting material filling the at least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and

a plurality of electronic components attached to the printed wiring board.

B6

68. A parallel joining technology method for making a multi-layer electronic interconnect structure, the method comprising:

B7

providing a layer of dielectric material bonded to a layer of electrically conductive material, the layer of dielectric material having substantially uniform thickness;

forming at least one passage through the layer of dielectric material to expose a portion of the layer of electrically conductive material;

depositing electrically conducting material in at least one of the at least one passage through the layer of dielectric material, such that the electrically conducting material in the at least one passage is in electrical contact with the layer of electrically conducting material bonded to the layer of dielectric material and extends beyond a surface of the layer of dielectric material;

removing portions of the layer of electrically conducting material to define a pattern of circuit conductors, such that at least one of the circuit conductors remains electrically connected to the electrically conductive material deposited in that at least one of the at least one passage through the layer of dielectric material;

stacking and aligning a plurality of structures comprising the layer of dielectric material with circuit conductors disposed thereon and conductively filled passages therethrough such that one of the following conditions exists:

a) at least one conductively filled passage in a structure contacts at least one circuit conductor on the conductive layer of an adjacent structure,

b) at least one circuit conductor on the conductive layer of a structure contacts at least one conductively filled passage in an adjacent structure, or

c) at least one conductively filled passage in a structure contacts at least one conductively filed passage in an adjacent structure;

forming a metallurgical bond thereby electrically and mechanically joining the electrically conductive material filled one of the at least one passage that is aligned with an electrically conductive feature on an adjacent structure to the adjacent structure conductive features; and

filling spaces between the adjacent structures with an electrically insulating material.